

Reversible Arithmetic Logic Gate (ALG) for Quantum Computation

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Abstract: At present, Boolean algebra based computations by the use of silicon based semiconductor technology are irreversible in nature. This is due to the mismatch of number of inputs and outputs. Reversible logic circuit maps unique input to the output and ensure one to one mapping and basis for emerging applications like low-power design, quantum computation, optical computing, bioinformatics and nanotechnologies. In computing paradigm, Arithmetic Logic Unit (ALU) is one of the computing intensive building blocks of the computer that performs arithmetic and logical operations. This work understands and nurtures the necessity of reversible ALU for future revolutionary computing technologies. In this paper, a 4x4 reversible gate which alone performs arithmetic and logic operations is proposed and compared with other reversible gates like TSG, HNG and MKG, in terms of quantum cost, I/O lines and Toffoli gates. The results of different synthesis methods of 4x4 ALG using Revkit tool are studied. Proposed gate performs better than existing methods and ensures maximum logical operations like full adder, full subtractor and all logical operations with less hardware cost where other existing gates are not viable.

Keywords: Arithmetic logic; Low Power Electronic design; Quantum computation; Reversible Logic; Reversible Synthesis.

1. Introduction

Moore's law describes a long-term trend in the history of computing hardware: the number of transistors that can be placed inexpensively on an integrated circuit doubles approximately every two years. Then the year 2020 or 2030 will find the circuits on an Integrated circuit measured on an atomic scale. As more and more logic elements into smaller and smaller volumes and clock them at higher and higher frequencies, more heat will be dissipated. This creates at least three problems: Energy costs money, Portable systems exhaust their batteries and Systems overheat. When a computational system erases a bit of information, it must dissipate $\ln 2 \times kT$ energy, where k is Boltzmann's constant and T is the temperature.

For $T = 300$ Kelvins (room temperature), this is

about 2.9×10^{-21} joules. This is roughly the kinetic energy of a single air molecule at room temperature. Today's computers erase a bit of information every time they perform a logic operation. These logic operations are therefore called "irreversible". This erasure is done very inefficiently, and much more than kT is dissipated for each bit erased. And the logical next step will be to create quantum computers, which will harness the power of atoms and molecules to perform memory and processing tasks. Quantum computers have the potential to perform certain calculations significantly faster than any silicon-based computer. A quantum computer is a device for computation that makes direct use of quantum mechanical phenomena, such as superposition and entanglement, to perform operations on data. Quantum computers are different from digital computers based on transistors. Whereas

digital computers require data to be encoded into binary digits (bits), quantum computation utilizes quantum properties to represent data and perform operations on these data. In this scenario, Reversible logic will play a vital role in transforming classical computation techniques into Quantum computation due to its reversible characteristics. These are called reversible logic operations, and in principle they can dissipate arbitrarily little heat. As the energy dissipated per irreversible logic operation approaches the fundamental limit of $\ln 2 \times kT$, the use of *reversible* operations is likely to become more attractive. In this paper, a novel four input reversible logic gate is proposed which exhibits less quantum cost and garbage outputs for a high computation intensive process like Arithmetic and Logic Operations. With this reason, we call the proposed gate as Arithmetic Logic Gate (ALG) and its important benchmarks are compared and discussed. The invention of new gate is mainly towards inventing new universal gate to optimize Arithmetic and logic design in a specific technology. Certain preferable properties of the already known gates are extended by following standard synthesis methods. ALG is a universal gate suitable for cost effective Arithmetic and Logic operations for future Quantum computation. Proposed gate is compared with the existing 4×4 TSG, HNG and MKG gates using the synthesis results obtained from the tool Revkit 1.1.2. Exact Synthesis(ES), Transformation Based (TB) synthesis and Binary Decision Diagram(BDD) are the synthesis techniques followed in this work to validate the proposed ALG gate. The rest of the paper is organized as follows. Section II summarizes the related work on reversible logic and gates. Section III deals with the background knowledge about basic reversible logic gates. Section IV presents the synthesis techniques considered in this work to validate the proposed ALG gate. Existing 4×4 gates and their Quantum circuits are presented in Section V. The proposed ALG gate is described in the Section VI. Section VII discusses the different synthesis results using Revkit. Finally, Section VIII concludes the paper.

2. Related Work

A Boolean function is called reversible if it maps each input assignment to a unique output assignment. Conventional irreversible logic gates leads to energy dissipation, regardless of the underlying circuit [1]. Research in this area is motivated by its promising potential on energy lossless circuit design [2], low-power CMOS design [3] quantum computation [4],

nanotechnology [5], etc. Bennett [6] further showed that zero energy dissipation is possible only if the circuit contains reversible gates. Reversible logic features a one-to one input output correspondence, which requires an equal number of inputs and outputs. Fan-outs and feedbacks are not allowed. These criteria make reversible logic synthesis a more challenging one. Exact synthesis methods, using Boolean satisfiability (SAT) [7], quantified Boolean formula (QBF) [8], dynamic programming [9], symbolic reachability [10], etc., can provide optimal solutions. In recent days, research in the area of reversible logic has been intensified and accelerated by the promising results. As a result, besides verification [11-13], testing [14-16], simulation [17, 18], optimization [19], and debugging [20] and synthesis of reversible circuits [7], approaches exploiting permutations and truth tables [21] are main research areas. Minimizing the number of garbage outputs and number of gates are the major concerns in reversible logic circuits and it is observed that proposed 4 input ALG gate achieves minimum garbage output and leading to high speed and low power reversible circuits. And the proposed 4 input ALG gate is compared with recently proposed 4 input gates TSG [22], HNG[23] and MKG[24] gates in terms of Quantum cost, Number of gates and number of lines. Another challenging direction in this domain is synthesis of reversible logic circuits. In this paper, we considered Exact [25, 26], Binary Decision Diagram (BDD)[27] and Transformation[28] based synthesis methods to analyze the proposed ALG gate's advantages over the existing ones.

3. Reversible Quantum Gates

Quantum gates are usually represented as matrices. A gate which acts on k qubits is represented by a $2^k \times 2^k$ unitary matrix. The number of qubits in the input and output of the gate have to be equal. The action of the quantum gate is found by multiplying the matrix representing the gate with the vector which represents the quantum state. In this section, some of the classical gates are classified in terms of number of inputs and presented.

3.1 Single qubit gates

3.1.1 Hadamard gate

The Hadamard gate acts on a single qubit. It maps the basis state $|0\rangle$ to $\frac{|0\rangle+|1\rangle}{\sqrt{2}}$ and $|1\rangle$ to $\frac{|0\rangle-|1\rangle}{\sqrt{2}}$ and represents a rotation of π about the x- and z-axes. It is represented by the Hadamard matrix:

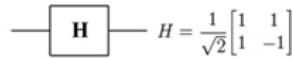


Figure 1 Hadamard gate

Since the rows of the matrix are orthogonal, **H** is indeed a unitary matrix.

3.1.2 Pauli-X gate

The Pauli-X gate acts on a single qubit. It is the quantum equivalent of a NOT gate. It equates to a rotation of the Bloch Sphere around the X-axis by π radians. It maps $|0\rangle$ to $|1\rangle$ and $|1\rangle$ to $|0\rangle$. It is represented by the Pauli X matrix:

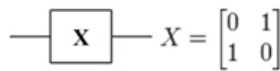


Figure 2 Pauli-X gate

3.1.3 Pauli-Y gate

The Pauli-Y gate acts on a single qubit. It equates to a rotation around the Y-axis of the Bloch Sphere by π radians. It maps $|0\rangle$ to $i|1\rangle$ and $|1\rangle$ to $-i|0\rangle$. It is represented by the Pauli Y matrix:

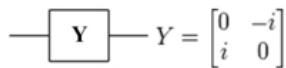


Figure 3 Pauli-Y gate

3.1.4 Pauli-Z gate

The Pauli-Z gate acts on a single qubit. It equates to a rotation around the Z-axis of the Bloch Sphere by π radians. Thus, it is a special case of a phase shift gate with $\theta = \pi$. It leaves the basis state $|0\rangle$ unchanged and maps $|1\rangle$ to $-|1\rangle$. It is represented by the Pauli Z matrix (Figure 4).

Since the rows of the matrix are orthogonal, **H** is indeed a unitary matrix.

3.2 2 * 2 Gates

3.2.1 Feynman gates

An example of a permutation gate is the Feynman gate (called also CNOT gate or Quantum XOR) shown in Figure 5. This gate can be described by the following logic expressions: $(A, B) \Rightarrow (P, Q) = (A, A \oplus B)$. This equation means that the output bit P is just the same as its input A, while on the output of the second wire Q the operation $A \oplus B$ is performed. This operation (EXOR of A and B) is a standard logic operation. A linear gate is one that all its outputs are

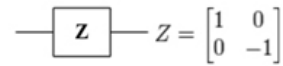


Figure 4 Pauli-Z gate

linear functions of input variables. Let a, b , and c be the inputs and P, Q and R the outputs of a gate. Assuming $2 * 2$ Feynman gate, $P = a, Q = a \oplus b$, when $a = 0$ then $Q = b$; when $a = 1$ then $Q = -b$. Feynman gate is used as a *fan-out (or copying)* gate. Two qubit permutation gates are resented in this section permutation gates. Every linear reversible function can be built by composing only $2 * 2$ Feynman gates and inverters. There exist $8! = 40,320$ $3 * 3$ reversible logic gates, some of them with interesting properties.

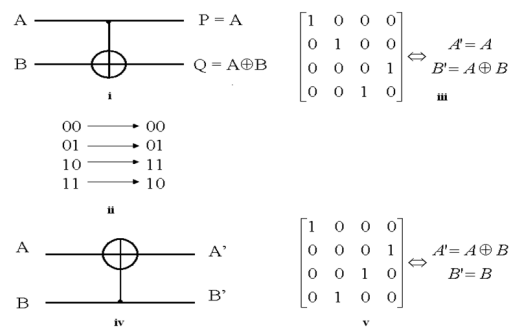


Figure 5 Feynman gates: (i) the circuit in quantum array notation, (ii) the transformation between states executed by this gate, (iii) the unitary matrix with binary enumeration of rows and columns and the corresponding Boolean equation of outputs, (iv) Feynman EXOR up circuit schematics, (v) its unitary matrix and Boolean equations

3.2.2 SWAP gate

Figure 6 presents another permutation gate called a Swap gate. Swap gate swaps the wires A and B, since input state 01 is transformed to output combination 10, input vector 10 is transformed to output vector 01 and the remaining combinations are unchanged.

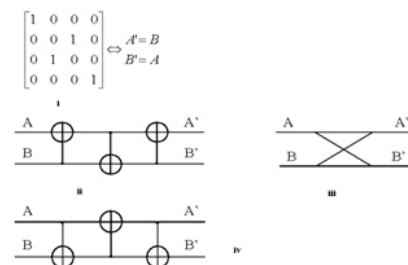


Figure 6 Swap gate: (i) unitary matrix and corresponding Boolean equations, (ii) realization using Feynman gates, (iii) a schematic, (iv) Realization using two Feynman gates and one Feynman EXOR up gate.

3.3 3 * 3 Gates

There exist two well-known universal 3 * 3 reversible gates [30]: Fredkin gate and Toffoli gate. Toffoli gate is also called 3 * 3 Feynman gate or Controlled-Controlled-NOT.

3.3.1 Toffoli gate

Toffoli gate is also called 3 * 3 Feynman gate or Controlled-Controlled-NOT (Figure 7). The 3 * 3 Toffoli gate is described by these equations:

$$P = a, Q = b, R = ab \oplus c.$$

Toffoli gate is an example of two-through gates, because two of its inputs are given to the output. Similarly, the concept of k-through gates can be introduced, as well as the concept of k * k Toffoli Gates. In general, for a reversible gate with n inputs and n outputs, the matrix is of size 2^n * 2^n.

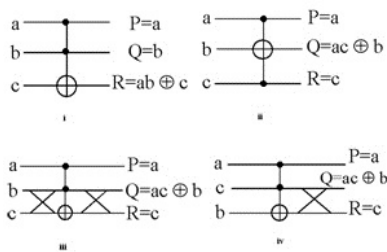


Figure 7 Toffoli gates: (i) a schematic of Toffoli gate (EXOR down), (ii) Toffoli gate (EXOR middle), (iii) realization of schematics from Figure (ii) using the Toffoli EXOR down and two Swap gates, (iv) realization of Toffoli EXOR middle with permuted input order

3.3.2 Fredkin gate

The 3 * 3 Fredkin gate (Figure 8) is described by these equations:

$$P = a, Q = \text{if } a \text{ then } c \text{ else } b, R = \text{if } a \text{ then } b \text{ else } c.$$

As we see, in terms of classical logic this gate is just two multiplexers controlled in a flipped (permuted) way from the same control input a. The symbol notation for a 3 * 3 Fredkin Gate is shown in Figure 8 i. Qubit a is the controlling qubit. A classical schematic of this gate that uses multiplexers is shown in Figure 8 ii. As we see, the 3 * 3 Fredkin gates are permutation gates, they permute the data inputs b,c of the multiplexers under control of the control input a of these multiplexers that is also outputted from the gate. Figure 8 iii presents a Fredkin gate controlled with qubit c. In Figure 8 iv qubit b is the controlling qubit.

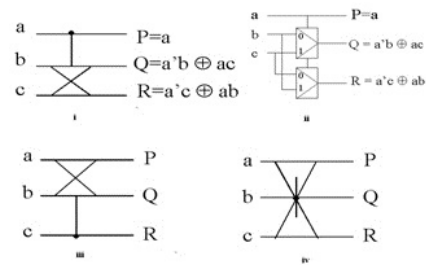


Figure 8 Fredkin gates: (i) Schematics with controlled qubit a, (ii) the classical schematics of this gate using multiplexers, (iii) Fredkin gate controlled by qubit c (Fredkin Down), (iv) Fredkin gate controlled by qubit b (Fredkin middle).

4. Reversible Logic Synthesis

Synthesis is the most important step while building complex circuits. Considering the traditional design flow, synthesis is carried out in several individual steps such as high-level synthesis, logic synthesis, mapping, and routing. This section briefly reviews existing methods for the reversible logic synthesis.

4.1 Exact synthesis method

The goal of the exact synthesis method [26] is to provide an algorithm for optimal synthesis of a reversible function, i.e. computing the minimal number of gates for a reversible function. The reversible cost of an implementation of a reversible function f is defined as the number of gates in the network representation that realizes f. This method [26] is based on reachability analysis [31] and uses Boolean Satisfiability based iterative algorithm. Hence a minimal solution is possible in the sense that there is no network realization with fewer gates. The basic idea is to check the existence of a Toffoli gate representation for the function with d gates, where d is increased in the next iteration if no realization is found. The number of Toffoli gates in n variables is determined.

4.2 Transformation based (TB) synthesis

A key factor of TB [28] is that the avoidance of extensive searching and therefore the method has greater potential to be extended to functions with more than just a few inputs and outputs. The synthesis problem is to find a sequence of Toffoli gates which transforms a given reversible function to the identity function. As gates can be applied either to the inputs or the outputs, the synthesis can proceed from outputs to inputs, inputs to outputs or in both directions simultaneously.

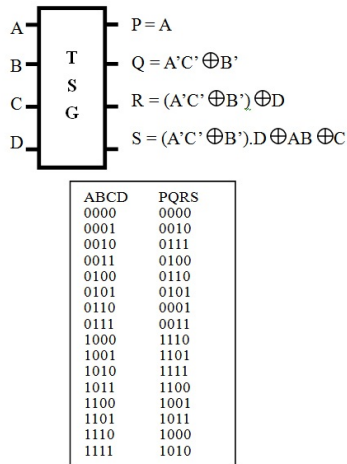


Figure 9 TSG Gate and its reversible one to one mapping

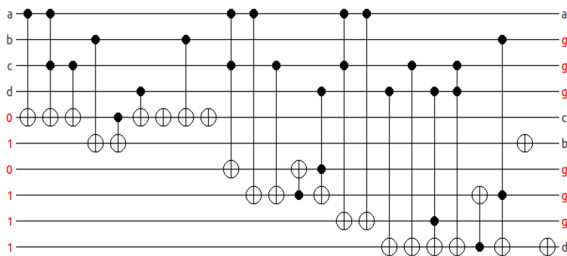


Figure 10 Quantum circuit of TSG gate (BDD Synthesis)

4.3 Binary decision diagram (BDD) synthesis

This is a synthesis technique to derive reversible circuits for a function given by a Binary Decision Diagram (BDD)[27]. The circuit is obtained using an algorithm with linear worst case behaviour regarding run-time and space requirements. Furthermore, the size of the resulting circuit is bounded by the BDD size. The basic idea is to create a Binary Decision Diagram for the function to be synthesized and afterwards substituting each node by a cascade of Toffoli or elementary quantum gates, respectively. BDD-based approach can synthesize larger circuits for functions with more than hundred variables in just a few CPU seconds.

5. Reversible Synthesis and Quantum Circuits of 4 * 4 Gates

In this section, existing 4 * 4 reversible gates, HNG, TSG, MKG are presented with their quantum circuits and synthesis results. Types of synthesis techniques considered are discussed in the section 4.

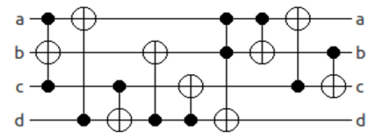


Figure 11 Quantum circuit of TSG gate (ES synthesis)

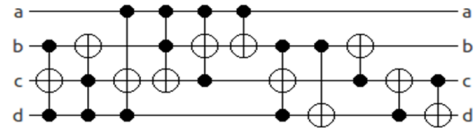


Figure 12 Quantum circuit of TSG gate (TB synthesis)

5.1 TSG gate

It is a four input reversible gate. The gate has unique one to one mapping. P output is A . Q output is $A'C' \oplus b'$. R output is $(A'C' \oplus b') \oplus D$. S output is $(A'C' \oplus b').D \oplus (AB \oplus C)$. I_v and O_v represent the input and output vectors respectively.

$$I_v = (A, B, C, D)$$

$$O_v = (P = A, Q = A'C' \oplus B', R = (A'C' \oplus B') \oplus D, S = (A'C' \oplus B').D \oplus AB \oplus C)$$

It can be verified that input pattern corresponding to a particular output pattern can be uniquely determined. The TSG gate is capable of implementing all Boolean functions and can also work singly as a reversible Full adder. The symbol for TSG gate and its one to one mapping are given by Figure 9. Quantum circuits of TSG gate using BDD, ES and TB synthesis are presented in Figure 10, 11 & 12 respectively. The gate has been used to construct Full adder, 4:2 compressor and Wallace tree multiplier [32].

5.2 HNG gate

It is a four input reversible gate. P output is A . Q output is B . R output is $A \oplus B \oplus C$. S output is $(A \oplus B)C \oplus (A \text{ AND } B) \oplus D$. I_v and O_v represent the input and output vectors respectively.

$$I_v = (A, B, C, D)$$

$$O_v = (P = A, Q = B, R = A \oplus B \oplus C, S = (A \oplus B)C \oplus AB \oplus D)$$

The symbol for HNG gate and its one to one mapping are given by Figure 13. Quantum circuits of HNG gate using BDD, ES and TB synthesis are presented in Figure 14, 15 & 16 respectively. One of the prominent functionalities of the HNG gate is that it can work singly as a reversible full adder [32]. Reversible full adder circuit uses only one reversible HNG gate. It produces only two garbage outputs. It requires

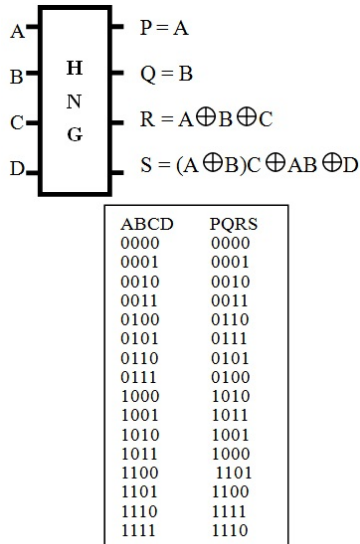


Figure 13 HNG gate and its one to one reversible mapping)

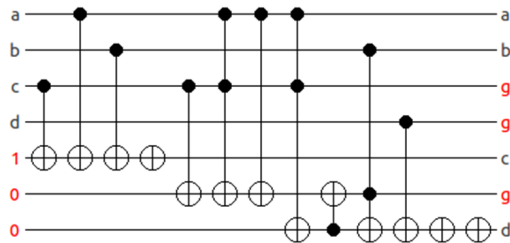


Figure 14 Quantum circuit of HNG gate (BDD synthesis)

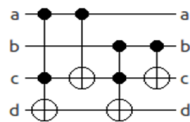


Figure 15 Quantum circuit of HNG gate (ES synthesis)

only one constant input and it needs only one clock cycle to perform the operations [32].

5.3 MKG gate

It is a four input reversible gate. A,B,C,D are inputs and P,Q,R,S are corresponding outputs. The gate has unique one to one mapping. P output is A. Q output is C. R output is $(A'D' \text{ XOR } B')$ XOR C. S output is $(A'D' \text{ XOR } B').C \text{ XOR } (AB \text{ XOR } D)$.

I_v and O_v represent the input and output vectors respectively.

$$I_v = (A, B, C, D)$$

$$O_v = (P = A, Q = C,$$

$$R = (A'D' \oplus B') \oplus C,$$

$$S = (A'D' \oplus B').C \oplus (AB \oplus D)$$

The symbol for MKG gate and its one to one map-

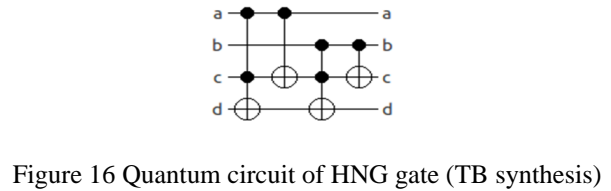


Figure 16 Quantum circuit of HNG gate (TB synthesis)

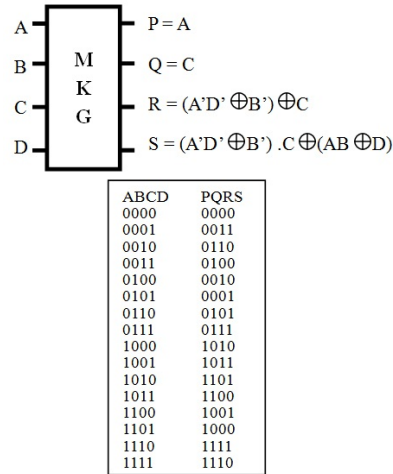


Figure 17 MKG gate and its one to one reversible mapping

ping are given by Figure 17. Quantum circuits of MKG gate using BDD, ES and TB synthesis are presented in Figure 18, 19 & 20. The MKG gate can be used to implement all Boolean functions. It also can be used to design efficient adders. One of the prominent functionalities of the MKG gate is that it can work singly as a reversible full adder unit, which is a versatile and widely used element in digital design.

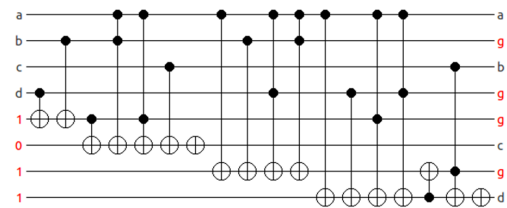


Figure 18 Quantum circuit of MKG (BDD synthesis)

6. Reversible Synthesis and Quantum Circuit of Proposed ALG Gate

The proposed gate is a four input reversible gate. A,B,C,D are inputs. P,Q,R,S are outputs. The symbol is given by Figure 21. I_v and O_v represent the input and output vectors respectively.

$$I_v = (A, B, C, D)$$

$$O_v = (P = A, Q = A \oplus B \oplus C,$$

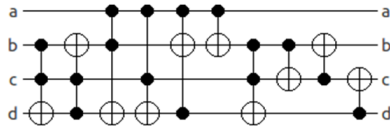


Figure 19 Quantum circuit of MKG (TB synthesis)

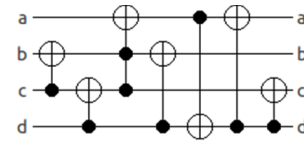


Figure 24 Quantum circuit of ALG (ES synthesis)

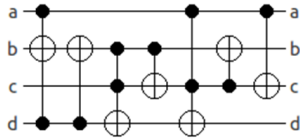


Figure 20 Quantum circuit of MKG (ES synthesis)

Table 1 List of arithmetic and logic functions

Condition	Input	Output
D=0	A,B,C	Q- Sum Difference, R- Carry, S-Borrow
D=1,C=0	A,B	Q- XOR, R-NAND, S-NOR
D=1,C=1	A,B	Q- XNOR, R- NOR, S-NAND

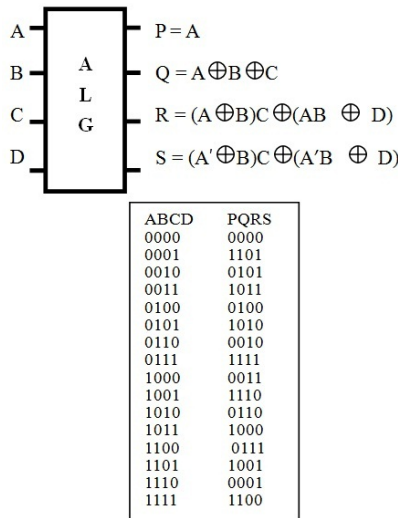


Figure 21 Proposed ALG Gate and its one to one reversible mapping

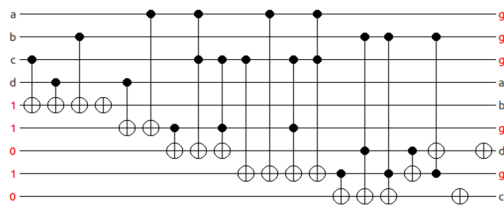


Figure 22 Quantum circuit of ALG (BDD synthesis)

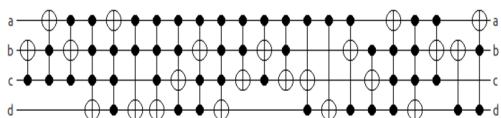


Figure 23 Quantum circuit of ALG (TB synthesis)

$$R = (A \oplus B)C \oplus (AB \oplus D),$$

$$S = (A' \oplus B)C \oplus (A'B \oplus D)$$

Functionalities of the gate

If $D = 0$, the proposed gate can act as full adder/full subtractor $O(P, Q, R, S) = fn(A, B, C)$

If $D = 1$ and $C = 0$, the proposed gate can function as logic function generator. Logic functions such as XOR, NAND, NOR functionalities can be realized.

$$O(P, Q, R, S) = fn(A, B)$$

7. Results & Discussion

The proposed ALG gate and existing is synthesised using BDD, TB and ES methods. Quantum cost, and number of gates and input/output lines are considered as benchmarks to evaluate the proposed ALG gate with existing TSG, HNG and MKG gates. To achieve one bit arithmetic and logical operations using the existing reversible gates require more number of gates and consume more gate delay. Using proposed ALG gate, all possible arithmetic and logical operations with single gate is possible without any more gate delays. Added to this, proposed ALG gate performs with less number of Toffoli gates, quantum cost and number of input/output lines using BDD and ES synthesis. Proposed gate under performs in TB synthesis method and which can be ignored because BDD method is validated that is better performing synthesis technique than TB [27]. ALG gate can be substantiated in terms of number of gates which ensures less propagation delay compare to existing gates. In future, ALG reversible gate will be validated as a basic building logic of a reversible logic circuit. Due to its technology limitations, presently, traditional computing evolves by improving the parallelism [33][34]. In future, certain emerging computing like optical, quantum, bio-

Table 2 Validation of ALG reversible gate

Synthesis	Parameters	ALG	TSG[22]	MKG[24]	HNG[23]
ES[26]	Number of Gates	7	9	7	4
	Quantum Cost	11	17	19	12
	Lines	4	4	4	4
BDD[27]	Number of Gates	20	24	18	13
	Quantum Cost	48	52	46	25
	Lines	9	10	8	7
TB[28]	Number of Gates	22	11	10	4
	Quantum Cost	162	35	34	12
	Lines	4	4	4	4

inspired computing will adopt reversible logic. After more validation of ALG in larger circuits and enhancements, it can be practically realized using optical logical gates [35], quantum cellular automata [36], etc.

8. Conclusion

The objective of this work is to propose a fundamental computing block as reversible gate which will perform a vital role in emerging innovative computing techniques like quantum computation. ALU is identified as a building block which has more computing overhead than others in the irreversible domain. This work intended to propose a reversible logic gate which performs all possible arithmetic and logical operation with less quantum cost. Proposed ALG gate is one among the $16!$ permutations of 4×4 one to one logical mapping. ALG gate is validated by comparing with other 4×4 reversible gates (TSG, HNG and MKG) using the results of ES, TB and BDD synthesis techniques. Low quantum cost reversible circuits to build the emerging quantum computing machine can use the proposed ALG gate for better reversible performance. Proposed gate for the reversible arithmetic and logical operations will find its space in the revolutionary computing techniques like optical computing, bio inspired computing, etc.

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