

Synthesis and Analysis of a Switched-Capacitor-Based Battery Equalizer Using Level-Shift Circuits

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Abstract: A switched-capacitor-based battery equalizer using level-shift circuits is proposed in this paper. In conventional equalizers using diode switches, the threshold voltage of diode switches causes a decrease in power efficiency. Unlike conventional equalizers, the proposed equalizer alleviates the threshold-voltage-drop of switches by using level-shift circuits. Therefore, the proposed equalizer can improve power efficiency. The properties of the proposed equalizer were investigated through SPICE simulations, theoretical analyses and experiments. SPICE simulations showed that 1. the proposed equalizer can improve power efficiency more than 40 % when output load R_L is 1 k Ω and 2. theoretical results corresponded well with SPICE simulation results. Therefore, the derived theoretical formulas will be helpful to estimate circuit properties of switched-capacitor-based battery equalizers. Furthermore, the experiments showed that the proposed equalizer can offer higher cell voltage than the conventional equalizer. Therefore, the proposed equalizer can achieve high power efficiency.

Keywords: Battery equalizer; Switched capacitor circuits; Level shift circuits; Switching converters; Bootstrap circuits; Power converters

1. Introduction

In many engineering applications, battery cells connected in series are usually used, because many engineering applications require higher voltage than the voltage of a single battery cell. However, the characteristic of single cells within a battery string is different due to temperature gradients of the battery pack, manufacturing variations, and so on. Consequently, the capacity of the battery pack decreases, because the individual cells have the different states of charge. To make matters worse, the lifespan of batteries will decrease exponentially as the number of battery cells increases.

To solve this problem, battery equalization circuits

have been proposed to equalize the voltage of individual cells. In current research, the equalization techniques can be classified in consumable charge equalization scheme and inductor-based charge equalization scheme and capacitor-based charge equalization scheme [1]-[13]. Among others, consumable charge equalization is one of the simplest technique. By redirecting a portion of the charging current to equalizers, consumable charge equalization schemes prevent the occurrence of overcharging. However, this method causes unnecessary energy loss, because battery energy is wasted by equalizers. To improve power efficiency, inductor-based charge equalization schemes have been proposed [2]-[11]. For example, inductor-

based battery equalizers using forward converters, Cuk converters, buck-boost converters, etc. have been realized by Kutkut et al., Lee et al., and so on [2]-[11]. Unlike the consumable charge equalization scheme, the inductor-based charge equalization scheme charges each battery cell by reducing power difference between battery cells. However, the inductor-based battery equalizer is difficult to realize light weight and small size, because magnetic components such as inductors, transformers, and so on are required. For this reason, inductor-less battery equalizers have been proposed by Kimball et al., Uno et al., and so on [12, 13], where the switched-capacitor (SC) technique [14]-[25] provides an alternative to the inductor-based technique. Among others, the SC battery equalizer, which can be synthesized with diode switches, capacitors and an AC voltage source [13], can provide no flux of magnetic induction, simple circuit control, light weight, small size, and so on. However, the threshold voltage of diode switches causes a decrease in the voltage of individual cells, because the energy transfer is performed through diode switches. Therefore, the improvement of power efficiency is necessary for the conventional SC battery equalizer.

In this paper, a novel switched-capacitor-based battery equalizer is proposed. Unlike conventional SC battery equalizers using diode switches, the proposed equalizer employs power switches with driver circuits to equalize the voltage of individual cells. The driver circuit consists of a level shift circuit, a diode switch and a small capacitor. First, when AC input is negative, the small capacitor is charged with the voltage of battery cells through the diode switch. Then, when AC input is positive, the power switch is driven by connecting the small capacitor to a gate terminal through the level shift circuit. For this reason, the voltage drop of battery cells is alleviated by using power switches with driver circuits. Consequently, the proposed equalizer can realize higher power efficiency than the conventional inductor-less equalizer. Concerning the proposed converter, theoretical analyses, SPICE simulations and experiments are performed to investigate circuit properties.

2. Circuit Structure

2.1 Conventional Battery Equalizer

Figure 1 shows an example of the conventional equalizer using diode switches [13]. By using AC voltage source V_{in} , the conventional equalizer of Figure 1 makes the voltage of V_{b_k} ($k = 1, 2, 3$) equal. As

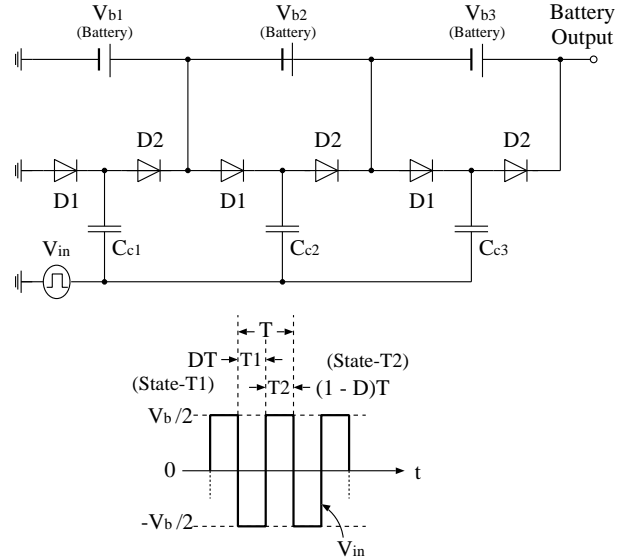


Figure 1. Conventional battery equalizer

shown in Figure 1, the interval of V_{in} is set to

$$T = T1 + T2, \quad T1 = DT$$

$$\text{and} \quad T2 = (1 - D)T, \quad (1)$$

where T is the period of V_{in} and D is the duty factor.

When input V_{in} is in *State - T1* (see in Figure 1), diode D_1 is turned on. Since capacitors C_{ck} ($k = 1, 2, 3$) is charged through D_1 , the voltage of capacitors C_{ck} , V_{ck} , is given by

$$V_{c1} = \frac{Vb}{2} - V_{th}, \quad V_{c2} = \frac{Vb}{2} - V_{th} + V_{b1}$$

$$\text{and} \quad V_{c3} = \frac{Vb}{2} - V_{th} + V_{b1} + V_{b2}, \quad (2)$$

where V_{th} denotes the threshold voltage of diode switches.

On the other hand, when input V_{in} is in *State - T2* (see in Figure 1), diode D_2 is turned on. Since capacitors C_{ck} is charged through D_2 , V_{ck} satisfies the following equations:

$$V_{b1} = V_{c1} - V_{th} + \frac{Vb}{2},$$

$$V_{b1} + V_{b2} = V_{c2} - V_{th} + \frac{Vb}{2}$$

$$\text{and} \quad V_{b1} + V_{b2} + V_{b3} = V_{c3} - V_{th} + \frac{Vb}{2}. \quad (3)$$

Therefore, from Eqs.(2) and (3), battery voltage V_{b_k} ($k = 1, 2, 3$) is given by

$$V_{b1} = V_{b2} = V_{b3} = Vb - 2V_{th}. \quad (4)$$

As Eq.(4) shows, the battery voltage is equalized. However, the voltage of each battery decreases due to the

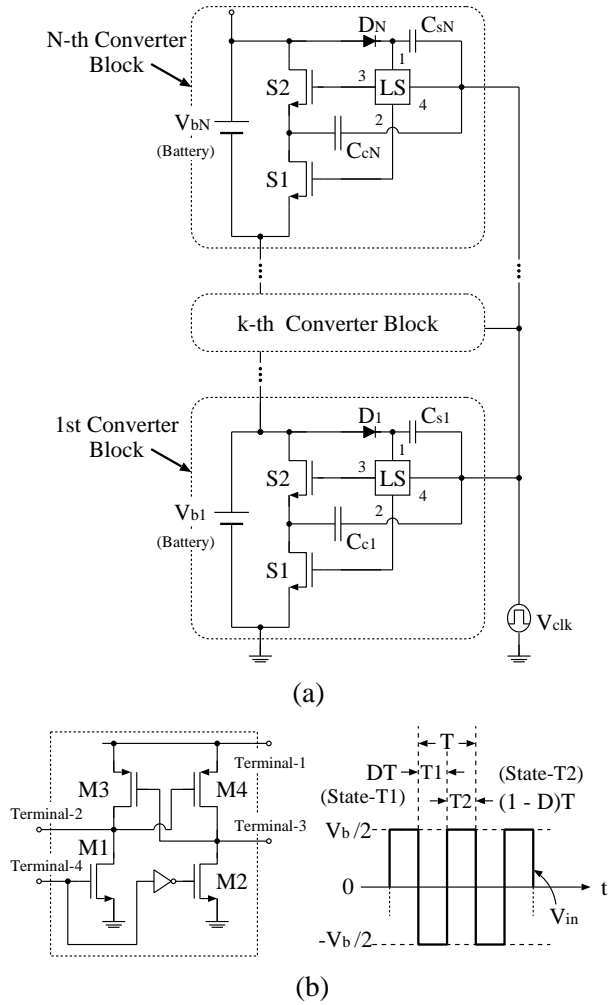


Figure 2. Proposed battery equalizer, (a) Proposed equalizer, (b) Level shift circuit

threshold voltage of diode switches. The threshold-voltage-drop causes a decrease in power efficiency.

2.2 Proposed Converter

Figure 2 shows the proposed battery equalizer. As Figure 2 shows, the proposed equalizer consists of N converter blocks. For easy understanding of the circuit operation, let us consider the k -th ($k = 1, \dots, N$) converter block.

When input V_{in} is in *State - T1*, transistors $M2$ and $M3$ in the level shift circuit are turned on. In this timing, power switch S_1 is turned on, because $Vb_k - V_{th}$ and 0 are outputted from the terminal-2 and the terminal-3, respectively. Since capacitor C_{ck} is charged through switch S_1 , V_{ck} satisfies the following equation:

$$V_{ck} = \frac{Vb}{2} + \sum_{i=1}^{k-1} Vb_i. \quad (5)$$

At the same time, capacitor C_{sk} is charged to $Vb_k - V_{th} + Vb/2$ through diode D_k .

On the other hand, when input V_{in} is in *State - T2*, transistors $M1$ and $M4$ in the level shift circuit are turned on. In this timing, power switch S_2 is turned on, because 0 and $Vb_k - V_{th} + Vb$ are outputted from the terminal-2 and the terminal-3, respectively. Since battery Vb_k is charged through switch S_2 , Vb_k satisfies the following equation:

$$\sum_{i=1}^k Vb_i = V_{ck} + \frac{Vb}{2}, \quad (6)$$

Therefore, from Eqs.(5) and (6), battery voltage Vb_k is given by

$$Vb_k = Vb. \quad (7)$$

As Eqs.(4) and (7) show, the proposed equalizer can alleviate the threshold-voltage-drop by using level-shift circuits. Therefore, the proposed converter can improve power efficiency.

The circuit properties of the proposed equalizer will be analyzed in the following section.

3. Theoretical Analysis

3.1 Proposed Equalizer

First, circuit properties of the proposed equalizer are analyzed. When the influence of driver circuits is negligibly small, the instantaneous equivalent circuits of the k -th converter block can be expressed as the circuits shown in Figure 3. In Figure 3, R_{on1} and R_{on2} denote on-resistances of power switches S_1 and S_2 , respectively.

In the steady state, differential value of the electric charge in capacitor C_{ck} satisfies

$$\Delta q_{T1}^{ck} + \Delta q_{T2}^{ck} = 0, \quad (8)$$

where Δq_{T1}^{ck} and Δq_{T2}^{ck} denote electric charges in the case of *State - T1* and *State - T2*, respectively. In the case of *State - T1*, differential values of electric charges in terminal V_{in} , terminal Vb_k and terminal Vb_{k-1} , $\Delta q_{V_{in},T1}$, $\Delta q_{Vb_k,T1}$ and $\Delta q_{Vb_{k-1},T1}$, are given by

$$\begin{aligned} \Delta q_{V_{in},T1} &= -\Delta q_{T1}^{ck}, \\ \Delta q_{Vb_k,T1} &= -\Delta q_{T1}^{bk} \\ \text{and } \Delta q_{Vb_{k-1},T1} &= -\Delta q_{T1}^{ck} - \Delta q_{T1}^{bk}. \end{aligned} \quad (9)$$

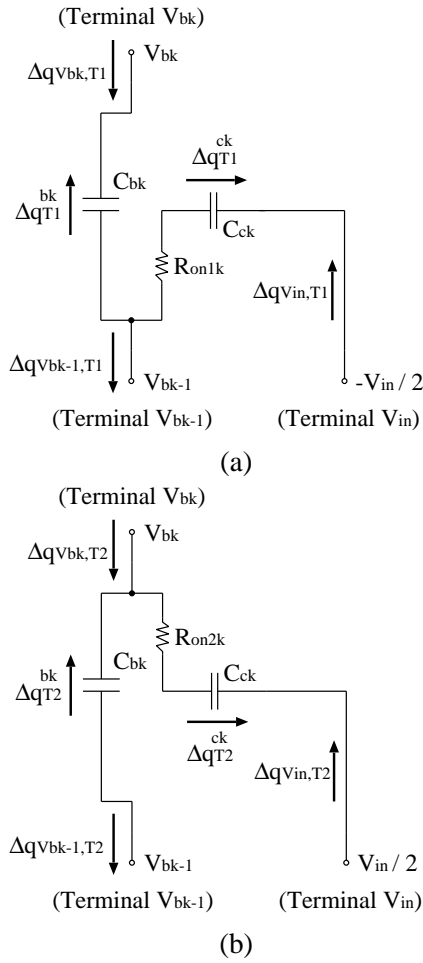


Figure 3. Instantaneous equivalent circuits of the k -th converter block, (a) *State - T1*, (b) *State - T2*

On the other hand, in the case of *State - T2*, differential values of electric charges in terminal V_{in} , terminal V_{b_k} and terminal $V_{b_{k-1}}$, $\Delta q_{V_{in},T2}$, $\Delta q_{V_{b_k},T2}$ and $\Delta q_{V_{b_{k-1}},T2}$, are given by

$$\begin{aligned} \Delta q_{V_{in},T2} &\equiv -\Delta q_{T2}^{ck}, \\ \Delta q_{V_{b_k},T2} &\equiv \Delta q_{T2}^{ck} - \Delta q_{T2}^{bk}, \\ \text{and } \Delta q_{V_{b_{k-1}},T2} &\equiv -\Delta q_{T2}^{bk}. \end{aligned} \quad (10)$$

Using Eqs.(9) and (10), differential values of electric charges in terminal V_{in} , terminal V_{b_k} and terminal $V_{b_{k-1}}$, $\Delta q_{V_{in}}$, $\Delta q_{V_{b_k}}$ and $\Delta q_{V_{b_{k-1}}}$, can be expressed as

$$\begin{aligned} \Delta q_{V_{in}} &\equiv -\Delta q_{V_{in},T1} + \Delta q_{V_{in},T2} \\ &\equiv 2\Delta q_{T1}^{ck}, \\ \Delta q_{V_{b_k}} &\equiv \Delta q_{V_{b_k},T1} + \Delta q_{V_{b_k},T2} \\ &\equiv -\Delta q_{T1}^{ck} \\ \text{and } \Delta q_{V_{b_{k-1}}} &\equiv \Delta q_{V_{b_{k-1}},T1} + \Delta q_{V_{b_{k-1}},T2} \\ &\equiv -\Delta q_{T1}^{ck}. \end{aligned} \quad (11)$$

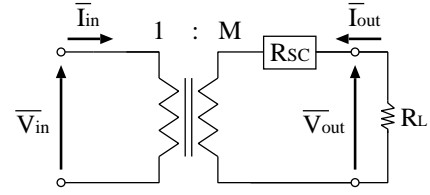


Figure 4. General form of the equivalent circuit

In Eqs.(11), the following equation is satisfied:

$$\Delta q_{V_{b_k}} = \Delta q_{V_{b_{k-1}}}, \quad (12)$$

because the converter blocks of the proposed converter are connected in series. Therefore, from Eqs.(11) and (12), we have the relation between average input current $\overline{I_{in}}$ and average output currents $\overline{I_{b_k}}$ and $\overline{I_{b_{k-1}}}$ as follows:

$$\overline{I_{in}} = -2\overline{I_{b_k}} = -2\overline{I_{b_{k-1}}}, \quad (13)$$

where

$$\begin{aligned} \overline{I_{in}} &\equiv \Delta q_{V_{in}}/T, \quad \overline{I_{b_k}} \equiv \Delta q_{V_{b_k}}/T \\ \text{and } \overline{I_{b_{k-1}}} &\equiv \Delta q_{V_{b_{k-1}}}/T. \end{aligned} \quad (14)$$

Next, let us consider the consumed energy of the k -th converter block in one period. In Figure 3, the consumed energy in one period, W_T , can be expressed as

$$W_T = W_{T1} + W_{T2}, \quad (15)$$

where

$$\begin{aligned} W_{T1} &= \frac{R_{on1k}}{T1} (\Delta q_{T1}^{ck})^2 \\ \text{and } W_{T2} &= \frac{R_{on2k}}{T2} (\Delta q_{T2}^{ck})^2. \end{aligned} \quad (16)$$

From Eqs.(8) ~ (12), Eq.(16) can be rewritten as

$$\begin{aligned} W_{T1} &= \frac{R_{on1k}}{DT} (\Delta q_{V_{b_k}})^2 \\ \text{and } W_{T2} &= \frac{R_{on2k}}{(1-D)T} (\Delta q_{V_{b_k}})^2. \end{aligned} \quad (17)$$

Here, a general equivalent circuit of SC power converters [22]-[25] can be given by the circuit shown in Figure 4. In Figure 4, R_{SC} denotes the SC resistance, M is the ratio of an ideal transformer, and $\overline{V_{in}}$ and $\overline{V_{out}}$ denote the average input voltage and the average output voltage, respectively. The consumed energy W_T in Figure 4 can be expressed as

$$\begin{aligned} W_T &= W_{T1} + W_{T2} \\ &\equiv \left(\frac{\Delta q_{V_{out}}}{T}\right)^2 \cdot R_{SC} \cdot T. \end{aligned} \quad (18)$$

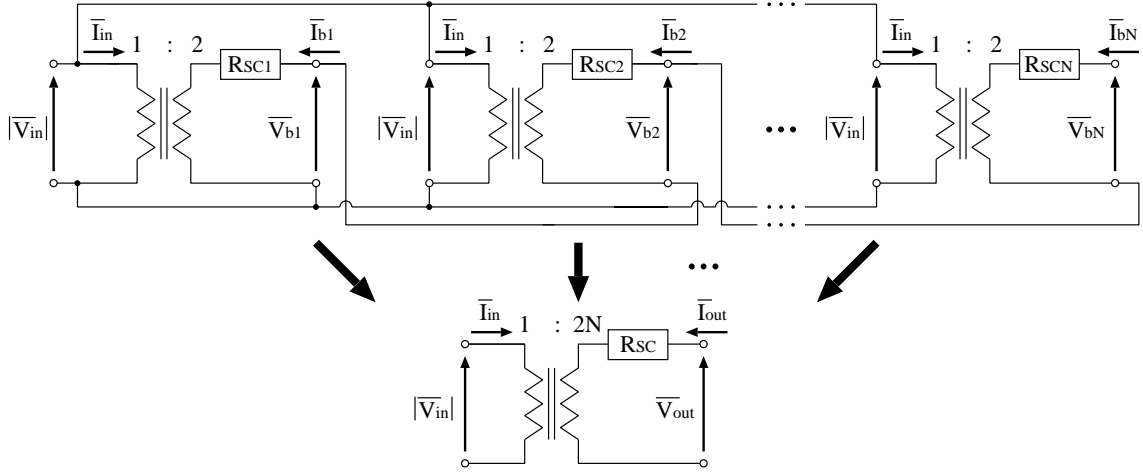


Figure 5. Equivalent circuit of the proposed equalizer

Substituting Eq.(17) into Eq.(18), we have the SC resistance R_{SCk} of the k -th converter block as follows:

$$R_{SCk} = \frac{(1-D)R_{on1k} + DR_{on2k}}{D(1-D)}. \quad (19)$$

Using Eqs.(13) and (19), the equivalent circuit of the k -th converter block can be expressed by the following determinant:

$$\begin{bmatrix} \overline{V_{in}} \\ \overline{I_{in}} \end{bmatrix} = \begin{bmatrix} 1/2 & 0 \\ 0 & 2 \end{bmatrix} \begin{bmatrix} 1 & R_{SCk} \\ 0 & 1 \end{bmatrix} \begin{bmatrix} \overline{V_{b_k}} \\ -\overline{I_{b_k}} \end{bmatrix}, \quad (20)$$

because the equivalent circuit shown in Figure 4 can be expressed by the determinant using the Kettenmatrix. As Eq.(20) shows, all the output voltage of the converter blocks becomes the same value if $R_{SC1} = \dots = R_{SCN}$. Finally, from Figure 2 and Eq.(20), we have the equivalent circuit of the proposed equalizer as shown in Figure 5. In Figure 5, R_{SC} , $\overline{V_{out}}$ and $\overline{I_{out}}$ denote

$$R_{SC} = \sum_{k=1}^N R_{SCk}, \quad \overline{V_{out}} = \sum_{k=1}^N \overline{V_{b_k}}$$

and $\overline{I_{out}} = \overline{I_{b_1}} = \dots = \overline{I_{b_N}}, \quad (21)$

respectively. From Figure 5, the power efficiency of the proposed equalizer can be expressed as

$$\eta = \frac{(\overline{I_{out}})^2 R_L}{(\overline{I_{out}})^2 R_{SC} + (\overline{I_{out}})^2 R_L} = \frac{R_L}{R_{SC} + R_L}, \quad (22)$$

where R_L denotes the output load.

3.2 Conventional Equalizer

In this subsection, circuit properties of the conventional equalizer shown in Figure 1 are analyzed. The instantaneous equivalent circuits of the conventional equalizer can be expressed as the circuits shown in Figure 6, where diode switch is modeled by an ideal switch, a voltage source V_{th} and a resistor R_{d1} (or R_{d2}). In Figure 6, V_{th} denotes the threshold voltage of diode switch, and R_{d1} and R_{d2} denote on-resistances of diode switches D_1 and D_2 , respectively.

In the steady state of Figure 6, differential value of the electric charge in capacitor C_{ck} satisfies Eq.(8). In the case of *State - T1*, differential values of electric charges in terminal V_{in} and terminal V_{b_k} ($k = 1, 2, 3$), $\Delta q_{V_{in},T1}$ and $\Delta q_{V_{b_k},T1}$, are given by

$$\begin{aligned} \Delta q_{V_{in},T1} &= -\Delta q_{T1}^c - \Delta q_{T1}^2 - \Delta q_{T1}^3, \\ \Delta q_{V_{b_1},T1} &= -\Delta q_{T1}^b, \\ \Delta q_{V_{b_2},T1} &= -\Delta q_{T1}^b, \\ \text{and } \Delta q_{V_{b_3},T1} &= -\Delta q_{T1}^b. \end{aligned} \quad (23)$$

On the other hand, in the case of *State - T2*, differential values of electric charges in terminal V_{in} and terminal V_{b_k} , $\Delta q_{V_{in},T2}$ and $\Delta q_{V_{b_k},T2}$, are given by

$$\begin{aligned} \Delta q_{V_{in},T2} &= -\Delta q_{T2}^c - \Delta q_{T2}^2 - \Delta q_{T2}^3, \\ \Delta q_{V_{b_1},T2} &= \Delta q_{T2}^c - \Delta q_{T2}^b, \\ \Delta q_{V_{b_2},T2} &= \Delta q_{T2}^c - \Delta q_{T2}^b, \\ \text{and } \Delta q_{V_{b_3},T2} &= \Delta q_{T2}^c - \Delta q_{T2}^b. \end{aligned} \quad (24)$$

Using Eqs.(23) and (24), differential values of electric charges in terminal V_{in} and terminal V_{b_k} , $\Delta q_{V_{in}}$ and $\Delta q_{V_{b_k}}$, can be expressed as

$$\Delta q_{V_{in}} \equiv -\Delta q_{V_{in},T1} + \Delta q_{V_{in},T2}$$

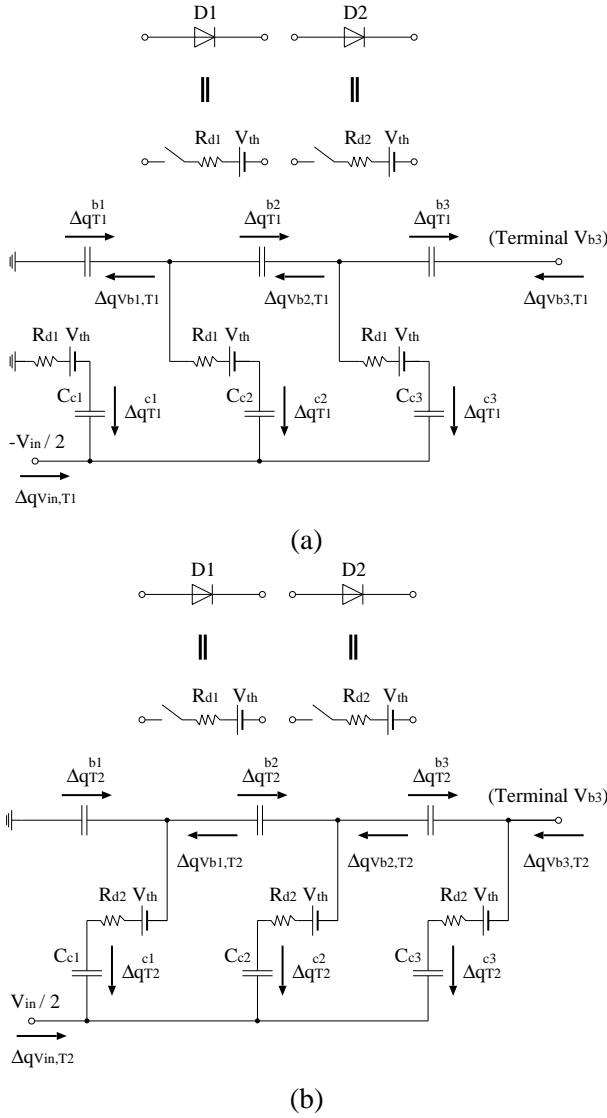


Figure 6. Instantaneous equivalent circuits of the conventional equalizer, (a) State – T1, (b) State – T2

$$\begin{aligned}
 &= 2(\Delta q_{T1}^{c1} + \Delta q_{T1}^{c2} + \Delta q_{T1}^{c3}), \\
 \Delta q_{Vb_1} &\equiv \Delta q_{Vb_1,T1} + \Delta q_{Vb_1,T2} \\
 &= -\Delta q_{T1}^{c1} \\
 \Delta q_{Vb_2} &\equiv \Delta q_{Vb_2,T1} + \Delta q_{Vb_2,T2} \\
 &= -\Delta q_{T1}^{c2} \\
 \text{and } \Delta q_{Vb_3} &\equiv \Delta q_{Vb_3,T1} + \Delta q_{Vb_3,T2} \\
 &= -\Delta q_{T1}^{c3}. \quad (25)
 \end{aligned}$$

In Eq.(25), the following equation is satisfied:

$$\Delta q_{Vb_1} = \Delta q_{Vb_2} = \Delta q_{Vb_3}, \quad (26)$$

because the converter blocks are connected in series (see Figure 1). Therefore, from Eqs.(24) and (25), we have the relation between average input current $\overline{I_{in}}$

and average output current $\overline{I_{b_k}}$ as follows:

$$\overline{I_{in}} = -6 \overline{I_{b_1}} = -6 \overline{I_{b_2}} = -6 \overline{I_{b_3}}, \quad (27)$$

where

$$\begin{aligned}
 \overline{I_{in}} &= \Delta q_{V_{in}}/T, & \overline{I_{b_1}} &= \Delta q_{V_{b_1}}/T, \\
 \overline{I_{b_2}} &= \Delta q_{V_{b_2}}/T \\
 \text{and } \overline{I_{b_3}} &= \Delta q_{V_{b_3}}/T. \quad (28)
 \end{aligned}$$

Next, let us consider the consumed energy in one period. In Figure 6, the consumed energy in one period, W_T , can be expressed as

$$W_T = W_{T1} + W_{T2}, \quad (29)$$

where

$$\begin{aligned}
 W_{T1} &= \frac{R_{d1}}{T1} (\Delta q_{T1}^{c1})^2 + \frac{R_{d1}}{T1} (\Delta q_{T1}^{c2})^2 \\
 &+ \frac{R_{d1}}{T1} (\Delta q_{T1}^{c3})^2 \\
 \text{and } W_{T2} &= \frac{R_{d2}}{T2} (\Delta q_{T2}^{c1})^2 + \frac{R_{d2}}{T2} (\Delta q_{T2}^{c2})^2 \\
 &+ \frac{R_{d2}}{T2} (\Delta q_{T2}^{c3})^2. \quad (30)
 \end{aligned}$$

From Eqs.(23) ~ (26), Eq.(30) can be rewritten as

$$\begin{aligned}
 W_{T1} &= \frac{3R_{d1}}{DT} (\Delta q_{V_{b_3}})^2 \\
 \text{and } W_{T2} &= \frac{3R_{d2}}{(1-D)T} (\Delta q_{V_{b_3}})^2. \quad (31)
 \end{aligned}$$

Substituting Eq.(31) into Eq.(18), SC resistance R_{SC} of the conventional equalizer is given by

$$R_{SC} = \frac{3(1-D)R_{d1} + 3DR_{d2}}{D(1-D)}, \quad (32)$$

because a general equivalent circuit of SC power converters can be expressed as the circuit shown in Figure 4. Using Eqs.(27) and (32), the equivalent circuit of the conventional equalizer is given by the following determinant:

$$\begin{aligned}
 &\begin{bmatrix} \overline{|V_{in}|} - V_{th} \\ \overline{I_{in}} \end{bmatrix} \\
 &= \begin{bmatrix} 1/6 & 0 \\ 0 & 6 \end{bmatrix} \begin{bmatrix} 1 & R_{SC} \\ 0 & 1 \end{bmatrix} \begin{bmatrix} \overline{V_{b_3}} \\ -\overline{I_{b_3}} \end{bmatrix}. \quad (33)
 \end{aligned}$$

Finally, using Eq.(33), the equivalent circuit of the conventional equalizer can be expressed as the circuit

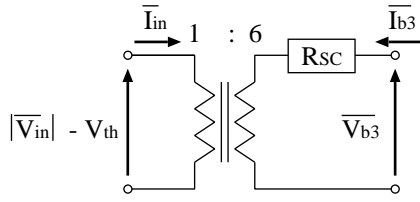


Figure 7. Equivalent circuit of the conventional equalizer

shown in Figure 7. From Figure 7, the power efficiency of the conventional equalizer can be expressed as

$$\begin{aligned} \eta &= \left(\frac{|V_{in}| - V_{th}}{|V_{in}|} \right) \times \frac{(\overline{I_{b3}})^2 R_L}{(\overline{I_{b3}})^2 R_{SC} + (\overline{I_{b3}})^2 R_L} \\ &= \left(\frac{|V_{in}| - V_{th}}{|V_{in}|} \right) \times \frac{R_L}{R_{SC} + R_L}. \end{aligned} \quad (34)$$

3.3 Comparison

From Eqs.(20), (21) and (22), the power efficiency of the proposed equalizer can be expressed as

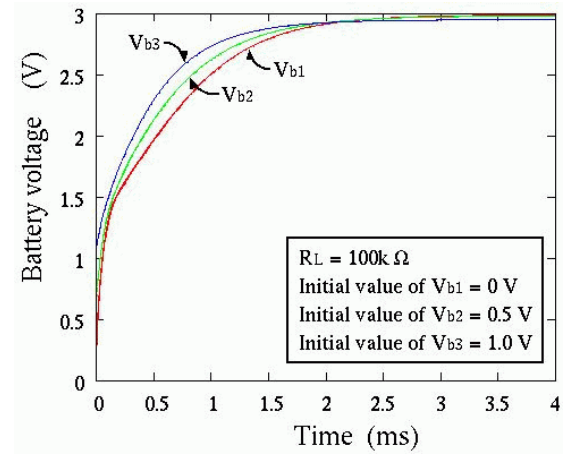
$$\eta = \frac{R_L}{12R_{on} + R_L} \quad (35)$$

if all the on-resistance of power switches is the same value R_{on} . On the other hand, from Eqs.(32) and (34), the power efficiency of the proposed equalizer can be expressed as

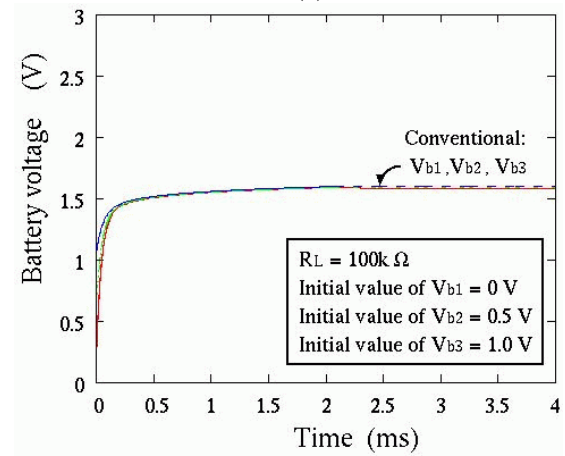
$$\eta = \left(\frac{|V_{in}| - V_{th}}{|V_{in}|} \right) \times \frac{R_L}{12R_d + R_L} \quad (36)$$

if all the on-resistance of diode switches is the same value R_d . As Eqs.(35) and (36) show, the proposed equalizer can improve the power efficiency from the conventional equalizer, because the power efficiency of the conventional equalizer decreases due to the threshold voltage of diode switches, and the on-resistance of diode switches is usually higher than that of power switches. To confirm the validity of theoretical analysis, the properties of the proposed equalizer with three converter blocks are investigated by SPICE simulations, where 0.35 μ m CMOS process was assumed to design the battery equalizer. SPICE simulations were performed under conditions where $V_{in} = \pm 1.5$ V @ 500 kHz, $C_{c1} = C_{c2} = C_{c3} = 5$ μ F, $C_{s1} = C_{s2} = C_{s3} = 10$ μ F, $C_{b1} = C_{b2} = C_{b3} = 100$ μ F¹, $D = 0.5$ and $R_{on1} = R_{on2} = 2$ Ω .

¹To investigate circuit properties of the proposed equalizer, capacitor $C_{bk} = 100$ μ F ($k = 1, 2, 3$) was used in substitution for battery V_{bk} ($k = 1, 2, 3$).



(a)



(b)

Figure 8. Simulated output voltages, (a) Proposed equalizer, (b) Conventional equalizer

Figure 8 shows the comparison of battery voltages between the proposed equalizer and the conventional equalizer shown in Figure 1. As Figure 8 shows, the proposed equalizer can equalize V_{bk} although the initial voltages of V_{bk} are different. Furthermore, the proposed equalizer can realize higher battery voltage than the conventional equalizer.

Figure 9 shows the power efficiency as a function of output load R_L . As Figure 9 shows, the theoretical result of the proposed equalizer corresponds well with simulated results. Therefore, the derived theoretical formulas will help us to estimate the characteristic of the battery equalizer. Furthermore, as Eqs.(22), (34) and Figure 9 show, the power efficiency of the proposed equalizer is higher than that of the conventional equalizer. Concretely, the proposed equalizer can improve power efficiency more than 40 % when output load R_L is 1 k Ω .

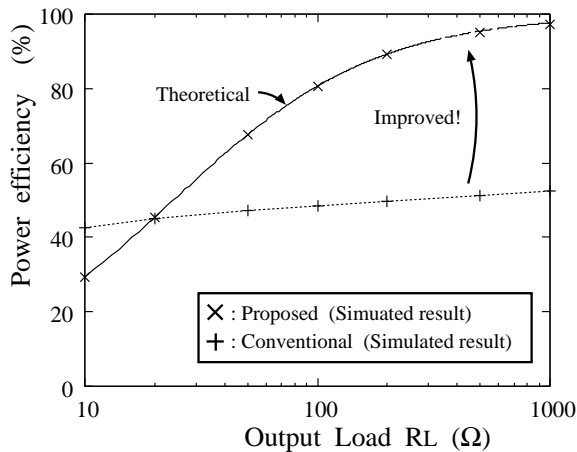


Figure 9. Power efficiency as a function of output load R_L

4. Conclusion

In this paper, a switched-capacitor-based battery equalizer using level-shift circuits has been proposed. The properties of the proposed equalizer were investigated through SPICE simulations and theoretical analyses.

The result of SPICE simulations showed that the proposed equalizer not only equalizes the voltage of batteries but also improves the power efficiency. Concretely, the proposed equalizer can improve power efficiency more than 40 % when output load R_L is 1 k Ω . Furthermore, the derived theoretical formulas can provide basic information to design switched-capacitor-based battery equalizers, because theoretical results corresponded with SPICE simulation results.

The IC implementation of the proposed equalizer is left to a future study.

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